An Area Efficient, High Performance, Low Dead Zone, Phase Frequency Detector in 180 nm CMOS Technology for Phase Locked Loop System

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Abstract: **The phase frequency detector has been designed for high frequency phase locked loop in 180 nm CMOS Technology with 1.8V supply voltage using CADENCE Spectre tool. A Virtuoso Analog Design Environment and Virtuoso LayoutXL tools of Cadence have used to design and simulate schematic and layout of phase frequency detector respectively. Architecture of phase frequency detector (PFD) has simulated to get low dead zone and low power consumption. A layout has designed by above tool and DRC by Assura. This circuit has designed with low power dissipation and small area .The total area required without pad is 0.06988 mm2 and current consumption is found to be 132.6 uA respectively.**

Index terms: **Phase locked loop (PLL), Phase frequency detector (PFD), Charge pump (CP), Voltage controlled oscillator (VCO), Dead Zone, Low pass filter (LPF), and D flip flop (DFF).**

I. Introduction

A PFD can detect the smallest phase difference of reference signal and output signal of VCO, because of this characteristic of the PFD it can be used as one of the important part of a PLL. The PLL consist of a PFD, LPF, CP and VCO. The PLL based on CP which is shown in figure 1 has been used because of its wide capture range and no phase offset. The operation of this circuit is basically a feedback control system that controls the phase of a VCO. The input signal is applied to one input of a phase frequency detector. The other input is taken from the divide by N counter.Now a day's PLLs are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizer in communication systems for clock extraction and generation of a low phase noise local oscillator. The phase difference between two input signals, i.e. the reference signal and the VCO output signal, can be processed by the PFD which is shown **in f**igure 2 for getting the phase error relative to the input and reference frequency. After detecting the phase error in terms of voltage, PFD can generate two signals named as UP and DN, which are connected to the charge pump circuit [1]. The output voltage of CP is used to control the output frequency of VCO. To tune according to output voltage of CP, the output value of PFD influences the output voltage of CP for VCO[2].

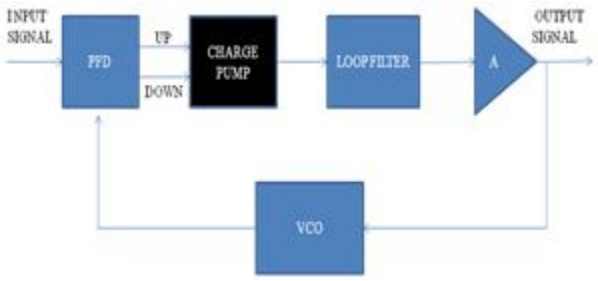

Figure 1. PLL Architecture

II. PFD Architecture

The traditional design consists of two D flip-flops and a NOR gate in the reset path to reset both the flip flop. The proposed schematic of the D flip flop (DFF) is shown in figure 3.The undetectable small phase range called as dead zone influences the effective sensitivity of a PFD.To minimize the power consumption of the PFD, it is must to reduce the reset path delay so that dead zone can be minimized. In order to avoid dead-zone a useful equation for the minimum reset delay of the PFD is given by equ.1.

$$T_{reset} = T_{th} = (Tr + T_{f)}/2 \quad \text{----------(1);}$$

Where T_{th} is the CP switching time and can be approximated by the average of the rise time T_r and the fall time T_f.To avoid a dead zone the minimum delay in the PFD reset path is $T_{reset} = T_{th}$ and the maximum delay in the PFD reset path is the maximum operating frequency of the PFD [3].The main reason of creation of static error at the output of the PLL is the long reset pulse which reduces the operating frequency of the PFD and the additional charges which are fed to the charge pump [4].The aim of this design is to reduce size and dead-zone because sensitivity of circuit is inversely proportional to the value of dead-zone [5].When delay time and reset time are large, a PFD cannot detect small phase error.

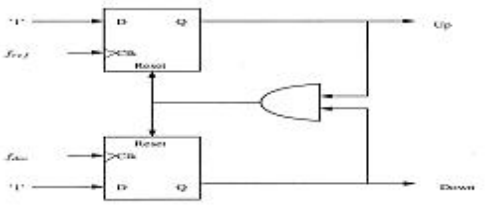

Figure 2. Block diagram of the PFD architecture

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The delay time of logic components and reset time of feedback path of flip-flop causes a PFD to detect phase and frequency with distortion [6].

III. Proposed PFD Architecture

To design PFD, two D flip flops along with a AND gate have been used. When CLK and RST signals applied to DFF's are at low level then drain node of NM4 (A) through pmos transistors PM4 and PM5 will be connected to V_{DD}.

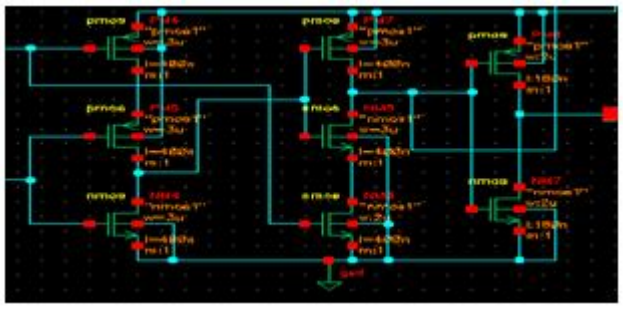

Figure 3. Schematic design of the D flip-flop.

At the rising edge of the CLK, Node B(drain of NM5) will be connected to ground through nmos transistor NM5 and NM6, because node 'A' is connected to V_{DD} which turns off pmos transistor PM7.Node A will be connected to the ground through nmos transistor NM4, which leads to pull up node B as RST signal charges up and it will become high due to switching ON of pmos transistor PM4.Transistor PM5 job is to prevent a short circuit in the PM4, PM5 and NM4 path. When CLK is at low level and RST is at high level, a large current w flows through this path. Therefore PM5 has been placed there to prevent this current and lower the power consumption of the D flip flop [7]. A AND gate has been used instead of NOR gate because NOR gate produces a large dead zone. In both these cases, different clock input to DFF, the subsequent rising-edge of the CLK causes the DN signal to lead the UP signal which causes a negative output increasing the phase and frequency difference. These kinds of malfunctions seriously degrade the locking property in PLLs [8].Such type of two DFFs are connected to implement a PFD with a AND gate as shown in Fig 2.The flip-flops have the same design, one of them will control the UP output of the PFD and the other will control the DOWN(DN) output. figure 3 shows schematic designs of the D flip flop. This type of rising edge detection connection for getting the phase detection scheme can be expanded further to reduce the bang-bang jitter. Compared with the binary detector, one NMOS is additionally required to pull-down the reset path [9].The UP and DN signals are fed to the charge pump to provide the control signal to VCO.A Large switch buffers are required in the CP to degrade the circuit noise performance for which a large transistors have been used.Large devices not only occupy larger chip area, but also slow down the circuit transient response [10].In order to increase the filtering effect for high-frequency and low-filter, a RC filter has been introduced. When RC filter pass band cut-off frequency is far greater than ten times of the loop bandwidth, impact of the RC filter to the stability of the loop is small [11].The divider logic divides the VCO frequency and output of divider logic sent to the phase frequency detector. The timing and phase of both can be compared by PFD and sent to CP which gives output in terms of a current pulse width which is equal to the amount of timing and phase error [12]. To achieve a high speed PFD, it is modified and another design is proposed which is shown in figure 4, which depends on detecting the rising and falling edge of the input signals [13].The non idealities in analog CMOS switches, such as charge injection and clock feed through periodically disturb the voltage on the LPF when it is off [14].In the PFD and CP circuits nonlinearity is mainly caused by the mismatch between the up and down currents and the gain variation. A maximum operation frequency is one over the shortest period with corrects UP and DN signals when the inputs have the same frequency and phase difference [15].Due to smaller node capacitances speed of the PFD increases. But due to finite delays of both D- flip flop and reset paths lead to a reduced linear range of its transfer characteristics. Therefore, it has high speed and fast acquisition [16].To implement higher speed PFD ,W/L of all transistors have been changed to reduce the node capacitances of transistors because the charge sharing phenomenon interchanges the control voltages of the PMOS transistors [17].A proposed PFD generating the UP and DN pulses according to the input applied to it .When CLK is applied with lagging to RST , number of UP pulses getting at the output of the PFD with lower width as compared to DN pulse width which is shown in Fig.5. However when CLK applied to PFD is lagging, number of pulses of DN signal getting at PFD with lower pulse width as compared to UP signal which is shown in figure 7.

IV. Result

The input clock frequency is 500 MHz with CLK leading RST by 4 ns this result in generation of an UP signal. The power consumption of the PFD is 2.08 mW @ 100 MHz which is a high value and that is due to the reset path that consumes some power to charge up and reset both flip-flops. Figure 5 and figure 6 shows a simulation of PFD at 100 MHz and CLK leading RST by 750 ps .The complete layout of the PFD is shown in Figure 7. The dead zone of the PFD can be reduced to 3 ps and which is shown in figure 6 and 7.The total layout area required for the PFD without pad is found to be is 0.06988 mm^2 and current consumption is found to be 132.6 uA respectively.

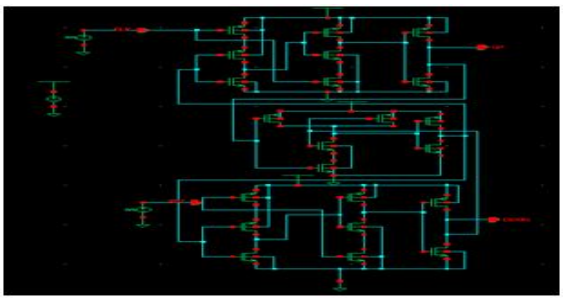

Figure 4. Proposed PFD Architecture

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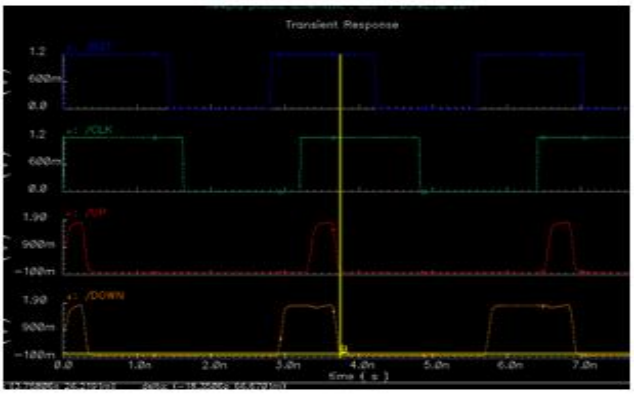

Figure 5. Output waveform of PFD when CLK is lagging

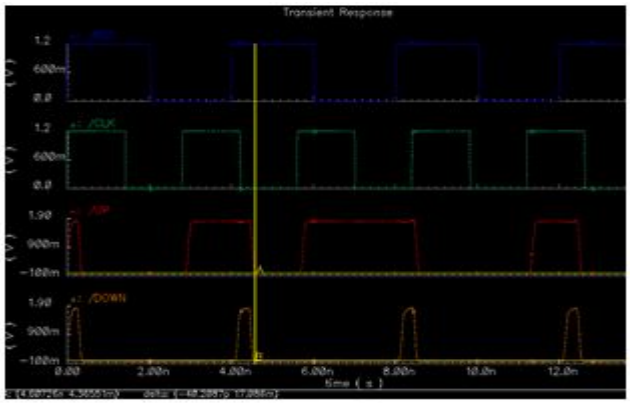

Figure 6. Output waveform of PFD with Dead Zone when CLK is leading

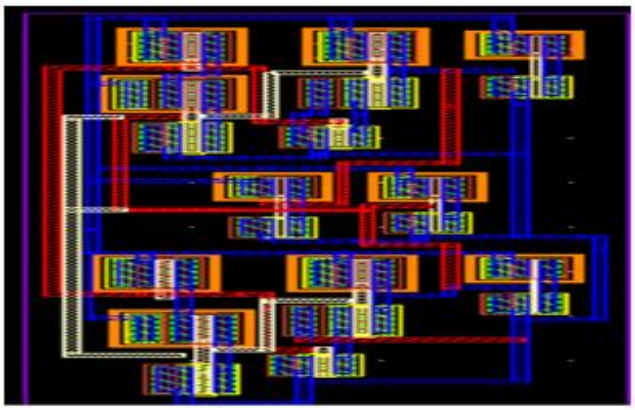

Figure 7. Layout of the PFD

V. Conclusion

The phase frequency detector has been designed to implement the PLL at 2.4 GHz and simulated by Virtuoso Cadence Spectre for low dead zone, small area and low power consumption. This circuit can be used in the application on high frequency, low dead zone and low power phase locked loop.

References

[1] N. H. E. Weste and K. Eshragrian, principles of CMOS VLSI Design, 2nd ed. MA Addison Wesley, 2001.

[2] Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

[3] Han-il Lee, Tae-won Ahn, Duck-young Jung and Byeong-ha Park," Scheme for No Dead Zone, Fast PFD Design", Journal of the Korean Physical Society, Vol. 40, No. 4, April 2002, pp. 543_545.

[4] Lip-Kai Soh, Yew-Fatt Kok Edwin, "An Adjustable Reset Pulse Phase Frequency Detector for Phase Locked Loop" Altera Corporation, Penang, Malaysia, ©2009 IEEE 343 1st Int'l Symposium on Quality Electronic Design-Asia

[5] Bianchi, Giovanni. Phase-Locked Loop Synthesizer Simulation. McGraw-Hill, 2005.

[6] Best, Roland E. Phase-Locked Loops Design, Simulation and Application. McGraw-Hill, 2003.

[7] Stephens, D. "Phase-Locked Loops for Wireless Communications Digital and Analog Implementations" Kluwer Academic Puplishers, 1998.

[8] Kun-Seok Lee*, Byeong-Ha Park, Han-il Lee, and Min Jong Yoh," Phase Frequency Detectors for Fast Frequency Acquisition in Zero-dead-zone CPPLLs for Mobile communication Systems " RF P/J, SYSTEM-LSI DIVISION, SAMSUNG ELECTRONICS, YONGIN, KYOUNGGI-DO, 449-711, KOREA.

[9] Young-Sang KIM, Yunjae SUH, Hong-June PARK, Jae-Yoon ,"Deadzone-Minimized Systematic Offset-Free Phase Detectors," SIM IEICE TRANS. ELECTRON., VOL.E91–C, NO.9 SEPTEMBER 2008,1525 LETTER.

[10] Ching-Lung Ti, Yao-Hong Liu and Tsung-Hsien Lin, " A 2.4-GHz Fractional-N PLL with a PFD/CP Linearization and an Improved CP Circuit", Graduate Institute of Electronics Engineering and Department of Electrical Engineering National Taiwan University

[11] Sun Wenyou, Hu Yonghong," Design and Realization of Direct PLL FM Transmitter for UAV Data Link", 2009 WASE International Conference on Information Engineering

[12] Xiang Gao, A. M. Klumperink, , Mounir Bohsali, and Bram Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied " JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 12, DECEMBER 2009 3253

[13] K. H. Cheng, T. H. Yao, S . Y. Jiang and W. B. Yang, "A Difference Detector PFD for Low Jitter PLL," Proceeding of the 8th IEEE Int. Conference on Circuits and Systems, vol. 1, pp. 43-46, Sept. 2001.

[14] Che-Fu Liang, Hsin-Hua Chen and Shen-Iuan Liu," Spur-Suppression Techniques for Frequency Synthesizers", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 54, NO. 8, AUGUST 2007.

[15] K. Arshak O. Abubaker E. Jafer,"Design and Simulation Difference Types CMOS Phase Frequency Detector for high speed and low jitter PLL", Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, Dominican Republic, Nov.3-5, 2004.

[16] I Ahmed, R D Mason,"A DUAL EDGE-TRIGGERED PHASE-FREQUENCY DETECTOR ARCHITECTURES", Department of Electronics, Carleton University, Ottawa, ON K1S 5B6, CANADA.

[17] R. Y. Chen and W.-Y. Chen,"A High-speed Fast-acquisition CMOS Phase/Frequency Detector for MB-OFDM UW", Manuscript received January 10, © 2007 IEEE.

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